

# OpenSTA

## Command Line Arguments

The command line arguments for `sta` are shown below.

```
sta [-help] [-version] [-no_init] [-f file]
  -help           show help and exit
  -version        show version and exit
  -no_init        do not read ~/.sta
  -no_splash     do not print the splash message
  -x cmd          evaluate cmd
  -f cmd_file    source cmd_file
  -threads count|max use count threads
```

When the STA starts up commands are first read from the user initialization file `~/.sta` if it exists. Next a command passed with the `-x` option is evaluated. Multiple commands can be specified in a quoted command string by separating them with semicolons. If a TCL command file is specified with `-f` on the command line, commands are read from the file and executed. Finally, a TCL command interpreter reads commands from standard input until the `exit` command is executed. The `-threads` option specifies how many parallel threads to use. Use `-threads max` to use one thread per processor.

A sample command file that reads a library and a Verilog netlist and reports timing checks is shown below.

```
read_liberty liberty.lib
read_verilog design.v
link_design top
create_clock -name clk -period 10 {clk1 clk2 clk3}
set_input_delay -clock clk 0 {in1 in2}
report_checks
```

Any number of Liberty and Verilog files can be read before linking the design. After linking the design, SDF or parasitics can be read.

An example command script using two process corners (ff and ss) is shown below.

```
read_liberty liberty.lib
read_verilog design.v
link_design top
define_corners ff ss
read_sdf -corner ff reg1.sdf
read_sdf -corner ss reg1_ss.sdf
create_clock -name clk -period 10 {clk1 clk2 clk3}
set_input_delay -clock clk 0 {in1 in2}
report_checks -path_delay min_max
report_checks -path_delay min_max -corner ss
report_checks -path_delay min_max -corner ff
```

## TCL Interpreter

Keyword arguments to commands may be abbreviated. For example,

```
report_checks -unique
```

is equivalent to the following command.

```
report_checks -unique_paths_to_endpoint
```

## Commands

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### **all\_clocks**

The **all\_clocks** command returns a list of all clocks that have been defined.

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### **all\_inputs**

The **all\_inputs** command returns a list of all input and bidirect ports of the current design.

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### **all\_outputs**

The **all\_outputs** command returns a list of all output and bidirect ports of the design.

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<b>all_registers</b>	<code>[-clock <i>clock_names</i>] [-cells] [-data_pins] [-clock_pins] [-async_pins] [-output_pins] [-level_sensitive] [-edge_triggered]</code>
<i>clock_names</i>	A list of <i>clock</i> names. Only registers clocked by these clocks are returned.
<code>-cells</code>	Return a list of register instances.
<code>-data_pins</code>	Return the register data pins.
<code>-clock_pins</code>	Return the register clock pins.
<code>-async_pins</code>	Return the register set/clear pins.
<code>-output_pins</code>	Return the register output pins.
<code>-level_sensitive</code>	Return level-sensitive latches.
<code>-edge_triggered</code>	Return edge-triggered registers.

The `all_registers` command returns a list of register instances or register pins in the design. Options allow the list of registers to be restricted in various ways. The `-clock` keyword restricts the registers to those that are clocked by a set of clocks. The `-cells` option returns the list of registers or latches (the default). The `-data_pins`, `-clock_pins`, `-async_pins` and `-output_pins` options cause `all_registers` to return a list of register pins rather than instances.

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<code>check_setup</code>	<code>[-verbose]</code> <code>[-unconstrained_endpoints]</code> <code>[-multiple_clock]</code> <code>[-no_clock]</code> <code>[-no_input_delay]</code> <code>[-loops]</code> <code>[-generated_clocks]</code> <code>[&gt; <i>filename</i>]</code> <code>[&gt;&gt; <i>filename</i>]</code>
<code>-verbose</code>	Show offending objects rather than just error counts.
<code>-unconstrained_endpoints</code>	Check path endpoints for timing constraints (timing check or <code>set_output_delay</code> ).
<code>-multiple_clock</code>	Check register/latch clock pins for multiple clocks.
<code>-no_clock</code>	Check register/latch clock pins for a clock.
<code>-no_input_delay</code>	Check for inputs that do not have a <code>set_input_delay</code> command.
<code>-loops</code>	Check for combinational logic loops.
<code>-generated_clocks</code>	Check that generated clock source pins have been defined as <code>clocks</code> .

The `check_setup` command performs sanity checks on the design. Individual checks can be performed with the keywords. If no check keywords are specified all checks are performed.

---

<code>connect_pins</code>	<code>net</code> <code>port_pin_list</code>
<code>net</code>	A net to add connections to.
<code>port_pin_list</code>	A list of ports or pins to connect to <code>net</code> ..

The `connect_pins` command connects ports or instance pins to a net.

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<b>create_clock</b>	-period period [-name <i>clock_name</i> ] [-waveform <i>edge_list</i> ] [-add] [ <i>pin_list</i> ]
<i>period</i>	The clock period.
<i>clock_name</i>	The name of the clock.
<i>edge_list</i>	A list of edge rise and fall time.
<i>-add</i>	Add this clock to the clocks on <i>pin_list</i> .
<i>pin_list</i>	A list of pins driven by the clock.

The `create_clock` command defines the waveform of a clock used by the design.

If no *pin\_list* is specified the clock is *virtual*. A virtual clock can be referred to by name in input arrival and departure time commands but is not attached to any pins in the design.

If no clock name is specified the name of the first pin is used as the clock name.

If a waveform is not specified the clock rises at zero and falls at half the clock period. The waveform is a list with time the clock rises as the first element and the time it falls as the second element.

If a clock is already defined on a pin the clock is redefined using the new clock parameters. If multiple clocks drive the same pin, use the `-add` option to prevent the existing definition from being overwritten.

The following command creates a clock with a period of 10 time units that rises at time 0 and falls at 5 time units on the pin named `clk1`.

```
create_clock -period 10 clk1
```

The following command creates a clock with a period of 10 time units that is high at time zero, falls at time 2 and rises at time 8. The clock drives three pins named `clk1`, `clk2`, and `clk3`.

```
create_clock -period 10 -waveform {8 2} -name clk {clk1 clk2 clk3}
```

<b>create_generated_clock</b>	<ul style="list-style-type: none"> <li><code>[-name <i>clock_name</i>]</code></li> <li><code>[-source <i>master_pin</i>]</code></li> <li><code>[-master_clock <i>master_clock</i>]</code></li> <li><code>[-pll_out <i>pll_out_pin</i>]</code></li> <li><code>[-pll_feedback <i>pll_fdbk_pin</i>]</code></li> <li><code>[-divide_by <i>divisor</i>]</code></li> <li><code>[-multiply_by <i>multiplier</i>]</code></li> <li><code>[-duty_cycle <i>duty_cycle</i>]</code></li> <li><code>[-invert]</code></li> <li><code>[-edges <i>edge_list</i>]</code></li> <li><code>[-edge_shift <i>shift_list</i>]</code></li> <li><code>[-add]</code></li> </ul> <p><i>pin_list</i></p>
<i>clock_name</i>	The name of the generated clock.
<i>master_pin</i>	A pin the the fanout of the master clock that is the source of the generated clock.
<i>master_clock</i>	The master clock used to generate the clock waveform.
<i>pll_out_pin</i>	The pin from <i>pin_list</i> that is the phase locked loop output pin.
<i>pll_fdbk_pin</i>	A pin in the fanout of the <i>pll_out_pin</i> that the phased locked loop phase locks to the master clock pin.
<i>divisor</i>	Divide the master clock period by <i>divisor</i> .
<i>multiplier</i>	Multiply the master clock period by <i>multiplier</i> .
<i>duty_cycle</i>	The percent of the period that the generated clock is high (between 0 and 100).
<code>-invert</code>	Invert the master clock.
<i>edge_list</i>	
<i>shift_list</i>	Not supported.
<code>-add</code>	Add this clock to the clocks on <i>pin_list</i> .
<i>pin_list</i>	A list of pins driven by the clock.

The `create_generated_clock` command is used to generate a clock from an existing clock definition. It is used to model clock generation circuits such as clock dividers and phase locked loops.

The `-source`, `-pll_out` and `-pll_feedback` must all be pins on the same PLL instance. The delay between the PLL out and feedback pins is removed from the source latency of the generated clock.

The `-divide_by`, `-multiply_by` and `-edges` arguments are mutually exclusive.

The `-multiply_by` option is used to generate a higher frequency clock from the source clock. The period of the generated clock is divided by *multiplier*. The clock *multiplier* must be a positive integer. If a duty cycle is specified the generated clock rises at zero and falls at period \* *duty\_cycle* / 100. If no duty cycle is specified the source clock edge times are divided by *multiplier*.

The `-divide_by` option is used to generate a lower frequency clock from the source clock. The clock *divisor* must be a positive integer. If the clock divisor is a power of two the source clock period is multiplied by *divisor*, the clock rise time is the same as the source clock, and the clock fall edge is one half period later. If the clock divisor is not a power of two the source clock waveform edge times are multiplied by *divisor*.

The `-edges` option forms the generated clock waveform by selecting edges from the source clock waveform.

If the `-invert` option is specified the waveform derived above is inverted.

If a clock is already defined on a pin the clock is redefined using the new clock parameters. If multiple clocks drive the same pin, use the `-add` option to prevent the existing definition from being overwritten.

In the example show below generates a clock named `gclk1` on register output pin `r1/Q` by dividing it by four.

```
create_clock -period 10 -waveform {1 8} clk1
create_generated_clock -name gclk1 -source clk1 -divide_by 4 r1/Q
```

The generated clock has a period of 40, rises at time 1 and falls at time 21.

In the example shown below the duty cycle is used to define the derived clock waveform.

```
create_generated_clock -name gclk1 -source clk1 -duty_cycle 50 \
                      -multiply_by 2 r1/Q
```

The generated clock has a period of 5, rises at time .5 and falls at time 3.

In the example shown below the first, third and fifth source clock edges are used to define the derived clock waveform.

```
create_generated_clock -name gclk1 -source clk1 -edges {1 3 5} r1/Q
```

The generated clock has a period of 20, rises at time 1 and falls at time 11.

---

<code>create_voltage_area</code>	<code>[-name name]</code>
	<code>[-coordinate coordinates]</code>
	<code>[-guard_band_x guard_x]</code>
	<code>[-guard_band_y guard_y]</code>
	<code>cells</code>

This command is parsed and ignored by timing analysis.

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<b>current_design</b>	<i>[design]</i>
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<b>current_instance</b>	<i>[instance]</i>
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<i>instance</i>	Not supported.
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<b>define_corners</b>	<i>corner_name1 [corner_name2]...</i>
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<i>corner_name</i>	The name of a delay calculation corner.
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Use the `define_corners` command to define the names of multiple process/temperature/voltage corners. The `define_corners` command must follow `set_operating_conditions -analysis_type` precede any reference to the corner names and can only appear once in a command file. There is no support for re-defining corners.

For analysis type `single`, each corner has one delay calculation result and early/late path arrivals. For analysis type `best_case/worst_case` and `on_chip_variation`, each corner has min/max delay calculation results and early/late path arrivals.

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<b>delete_instance</b>	<i>instance_list</i>
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<i>instance_list</i>	A list of instances to remove.
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The network editing command `delete_instance` removes an instance from the design.

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<b>delete_net</b>	<i>net_list</i>
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<i>net_list</i>	A list of nets to remove.
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The network editing command `delete_net` removes a net from the design.

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<b>disconnect_pins</b>	<i>net</i> <i>port_pin_list/-all</i>
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<i>net</i>	The net to disconnect pins from.
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<i>port_pin_list</i>	A list of ports or pins to disconnect from <i>net</i> .
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**-all** Disconnect all pins from the net.

Disconnects pins from a net. Parasitics connected to the pins are deleted.

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**elapsed\_run\_time**

Returns the total clock run time in seconds as a float.

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<b>find_timing_paths</b>	<code>[-from <i>from_list</i>    -rise_from <i>from_list</i>    -fall_from <i>from_list</i>] [-through <i>through_list</i>    -rise_through <i>through_list</i>    -fall_through <i>through_list</i>] [-to <i>to_list</i>    -rise_to <i>to_list</i>    -fall_to <i>to_list</i>] [-unconstrained] [-path_delay min min_rise min_fall    max max_rise max_fall    min_max] [-group_count <i>path_count</i>] [-endpoint_count <i>endpoint_path_count</i>] [-unique_paths_to_endpoint] [-corner <i>corner_name</i>] [-slack_max <i>max_slack</i>] [-slack_min <i>min_slack</i>] [-sort_by_slack] [-path_group <i>group_names</i>]</code>
<i>from_list</i>	A list of clocks, instances, ports or pins.
<i>through_list</i>	A list of instances, pins or nets.
<i>to_list</i>	A list of clocks, instances, ports or pins.
<b>-unconstrained</b>	Return unconstrained paths.
<b>-path_delay min</b>	Report min path (hold) checks.
<b>-path_delay min_rise</b>	Report min path (hold) checks for rising endpoints.
<b>-path_delay min_fall</b>	Report min path (hold) checks for falling endpoints.

<code>-path_delay max</code>	Report max path (setup) checks.
<code>-path_delay max_rise</code>	Report max path (setup) checks for rising endpoints.
<code>-path_delay max_fall</code>	Report max path (setup) checks for falling endpoints.
<code>-path_delay min_max</code>	Report max and min path (setup and hold) checks.
<code>path_count</code>	The number of paths to report in each path group.
<code>endpoint_path_count</code>	The number of paths to report for each endpoint.
<code>-unique_paths_to_endpoint</code>	Report multiple paths to an endpoint that traverse different pins without showing multiple paths with different rise/fall transitions.
<code>corner_name</code>	Only report paths for one process corner.
<code>max_slack</code>	Only report paths with less slack than <code>max_slack</code> .
<code>min_slack</code>	Only report paths with more slack than <code>min_slack</code> .
<code>-sort_by_slack</code>	Sort paths by slack rather than slack grouped by path group.
<code>group_names</code>	List of path group names to report. All path groups are reported if this option is not specified.

The `find_timing_paths` command returns a list of path objects for scripting. Use the `get_property` function to access properties of the paths.

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<code>get_cells</code>	<code>[-hierarchical] [-hsc separator] [-filter expr] [-regexp] [-nocase] [-quiet] [-of_objects objects] [patterns]</code>
<code>-hierarchical</code>	Searches hierarchy levels below the current instance for matches.
<code>separator</code>	Character to use to separate hierarchical instance names in <code>patterns</code> .

*expr*

A filter expression of the form  
attribute ==|~= pattern  
where attribute is an attribute supported by the  
get\_property command.

*objects*

The name of a pin or net, a list of pins returned by  
get\_pins, or a list of nets returned by get\_nets. The  
-hierarchical option cannot be used with -of\_objects.

*patterns*

A list of cell (instance) name patterns.

The `get_cells` command returns a list of all cell instances that match *patterns*.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression  
matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can  
only be used with `-regexp`.

---

**get\_clocks**

[-regexp]  
[-nocase]  
[-quiet]  
*patterns*

`-quiet`

Do not report an error if *patterns* do not match  
anything.

*patterns*

A list of clock name patterns.

The `get_clocks` command returns a list of all clocks that have been defined.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression  
matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can  
only be used with `-regexp`.

---

**get\_fanin**

-to *sink\_list*  
[-flat]  
[-only\_cells]  
[-startpoints\_only]  
[-levels *level\_count*]  
[-pin\_levels *pin\_count*]  
[-trace\_arcs timing|enabled|all]

<i>sink_list</i>	List of pins, ports, or nets to find the fanin of. For nets, the fanin of driver pins on the nets are returned.
<i>-flat</i>	Without <i>-flat</i> only pins at the same hierarchy level as the sinks are returned. With <i>-flat</i> pins in the fanin at any hierarchy level are returned.
<i>-only_cells</i>	Return the instances connected to the pins in the fanin.
<i>-startpoints_only</i>	Only return pins that are startpoints.
<i>level_count</i>	Only return pins within <i>level_count</i> instance traversals.
<i>pin_count</i>	Only return pins within <i>pin_count</i> pin traversals.
<i>-trace_arcs</i>	With 'timing' and 'enabled' values only arcs that are not disabled are traversed. With a value of 'all' even disabled arcs are traversed.

The `get_fanin` command returns traverses the design from *sink\_list* pins, ports or nets backwards and return the fanin pins or instances.

---

<b>get_fanout</b>	<code>-from source_list</code> <code>[-flat]</code> <code>[-only_cells]</code> <code>[-endpoints_only]</code> <code>[-levels level_count]</code> <code>[-pin_levels pin_count]</code> <code>[-trace_arcs timing enabled all]</code>
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<code>source_list</code>	List of pins, ports, or nets to find the fanout of. For nets, the fanout of load pins on the nets are returned.
<code>-flat</code>	Without <code>-flat</code> only pins at the same hierarchy level as the sinks are returned. With <code>-flat</code> pins in the fanout at any hierarchy level are returned.
<code>-only_cells</code>	Return the instances connected to the pins in the fanout.
<code>-endpoints_only</code>	Only return pins that are endpoints.
<code>level_count</code>	Only return pins within <code>level_count</code> instance traversals.
<code>pin_count</code>	Only return pins within <code>pin_count</code> pin traversals.
<code>-trace_arcs</code>	With 'timing' and 'enabled' values only arcs that are not disabled are traversed. With a value of 'all' even disabled arcs are traversed.

The `get_fanout` command returns traverses the design from `source_list` pins, ports or nets backwards and return the fanout pins or instances.

---

<code>get_lib_cells</code>	<code>[-of_objects objects]</code> <code>[-hsc separator]</code> <code>[-regexp]</code> <code>[-nocase]</code> <code>[-quiet]</code> <code>patterns</code>
<code>objects</code>	A list of cell (instance) objects.
<code>separator</code>	Character that separates the library name and cell name in <code>pattern</code> .
<code>-quiet</code>	Do not report an error if <code>patterns</code> do not match anything.
<code>patterns</code>	A list of library cell name patterns of the form <code>library_name/cell_name</code> .

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The `get_lib_cells` command returns a list of library cells that match `pattern`. The library name can be prepended to the cell name pattern with the `separator` character, which defaults to `hierarchy_separator`.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can only be used with `-regexp`.

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<b>get_lib_pins</b>	<code>[-hsc <i>separator</i>] [-regexp] [-nocase] [-quiet] <i>patterns</i></code>
<i>separator</i>	Character that separates the library name, cell name and port name in <i>pattern</i> .
<code>-quiet</code>	Do not report an error if <i>patterns</i> do not match anything.
<i>patterns</i>	A list of library port name patterns of the form library_name/cell_name/port_name.

The `get_lib_pins` command returns a list of library ports that match *pattern*. Use `separator` to separate the library and cell name patterns from the port name in *pattern*.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can only be used with `-regexp`.

---

<b>get_libs</b>	<code>[-regexp] [-nocase] [-quiet] <i>patterns</i></code>
<code>-quiet</code>	Do not report an error if <i>patterns</i> do not match anything.
<i>patterns</i>	A list of library name patterns.

The `get_libs` command returns a list of clocks that match *patterns*.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can only be used with `-regexp`.

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<b>get_nets</b>	<code>[-hierarchical] [-hsc <i>separator</i>] [-regexp] [-nocase] [-quiet] [-of_objects <i>objects</i>] [<i>patterns</i>]</code>
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<code>-hierarchical</code>	Searches hierarchy levels below the current instance for matches.
<code>separator</code>	Character that separates hierarchical instance names and the net name in <i>pattern</i> .
<code>-quiet</code>	Do not report an error if <i>patterns</i> do not match anything.
<code>objects</code>	The name of a pin or instance, a list of pins returned by <code>get_pins</code> , or a list of instances returned by <code>get_cells</code> . The <code>-hierarchical</code> option cannot be used with <code>-of_objects</code> .
<code>patterns</code>	A list of net name patterns.

The `get_nets` command returns a list of all nets that match *patterns*.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can only be used with `-regexp`.

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<code>get_full_name</code>	<i>object</i>
<i>object</i>	A library, cell, port, instance, pin or timing arc object.

Return the name of *object*. Equivalent to `[get_property object full_name]`.

---

<code>get_name</code>	<i>object</i>
<i>object</i>	A library, cell, port, instance, pin or timing arc object.

Return the name of *object*. Equivalent to `[get_property object name]`.

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<code>get_pins</code>	<code>[-hierarchical]</code> <code>[-hsc separator]</code> <code>[-filter expr]</code> <code>[-regexp]</code> <code>[-nocase]</code> <code>[-quiet]</code> <code>[-of_objects objects]</code> <code>[patterns]</code>
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<code>-hierarchical</code>	Searches hierarchy levels below the current instance for matches.
<code>separator</code>	Character that separates hierarchical instance names and the port name in <i>pattern</i> .
<code>-quiet</code>	Do not report an error if <i>patterns</i> do not match anything.
<code>expr</code>	A filter expression of the form $attribute == ~= pattern$ where <i>attribute</i> is an attribute supported by the <code>get_property</code> command.
<code>objects</code>	The name of a net or instance, a list of nets returned by <code>get_nets</code> , or a list of instances returned by <code>get_cells</code> . The <code>-hierarchical</code> option cannot be used with <code>-of_objects</code> .
<code>patterns</code>	A list of pin name patterns.

The `get_pins` command returns a list of all instance pins that match *patterns*.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can only be used with `-regexp`.

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<code>get_ports</code>	<code>[-filter expr]</code> <code>[-regexp]</code> <code>[-nocase]</code> <code>[-quiet]</code> <code>[-of_objects objects]</code> <code>[patterns]</code>
<code>-quiet</code>	Do not report an error if <i>patterns</i> do not match any clocks.
<code>expr</code>	A filter expression of the form $attribute == ~= pattern$ where <i>attribute</i> is an attribute supported by the <code>get_property</code> command.
<code>objects</code>	The name of a net, or a list of nets returned by <code>get_nets</code> .
<code>patterns</code>	A list of port name patterns.

The `get_ports` command returns a list of all top level ports that match *patterns*.

Without `-regexp` Unix style file glob pattern matching is used. With `-regexp` TCL regular expression matching is used. When `-nocase` is used regular expressions are case insensitive. The `-nocase` flag can only be used with `-regexp`.

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<code>get_property</code>	<code>[-object_type object_type]</code>
	<code>object</code>
	<code>property</code>
 <code>object_type</code>	<code>cell pin net port clock timing_arc</code>
 <code>object</code>	An object or object name if <code>-object_type</code> is specified.
 <code>property</code>	A property name.

The properties for different objects types are shown below.

`instance (cell)`

```
ref_name
full_name
```

`pin`

```
direction
full_name
lib_pin_name
clocks
actual_fall_transition_min
actual_fall_transition_max
actual_rise_transition_min
actual_rise_transition_max
min_fall_slack
max_fall_slack
min_rise_slack
max_rise_slack
```

`port`

```
direction
full_name
actual_fall_transition_min
actual_fall_transition_max
actual_rise_transition_min
actual_rise_transition_max
min_fall_slack
max_fall_slack
min_rise_slack
max_rise_slack
```

`net`

```
full_name
```

`liberty_port`

```
direction
full_name
```

```
liberty_cell
```

```
base_name
full_name
```

```
library
```

```
name
```

```
clock
```

```
name
period
sources
```

```
edge
```

```
delay_min_fall
delay_max_fall
delay_min_rise
delay_max_rise
```

```
path(PathEnd)
```

```
endpoint
endpoint_clock
endpoint_clock_pin
slack
startpoint
startpoint_clock
points
```

```
point (PathRef)
```

```
pin
arrival
required
slack
```

---

```
get_timing_edges           [-from from_pins]
                           [-to to_pins]
                           [-of_objects objects]
                           [-filter expr]
                           [patterns]
```

```
from_pin                  A collection of pins.
```

```
to_pin                   A collection of pins.
```

*objects* A collection of instances or library cells. The `-from` and `-to` options cannot be used with `-of_objects`.

*expr* A filter expression of the form  
    *attribute* `==|~=` *pattern*  
where *attribute* is an attribute supported by the `get_property` command.

The `get_timing_edges` command returns a collection of timing edges (arcs) to, from or between pins. The result can be passed to `get_property` or `set_disable_timing`.

---

<b>group_path</b>	<code>-name <i>group_name</i></code> [ <code>-weight <i>weight</i></code> ] [ <code>-critical_range <i>range</i></code> ] [ <code>-from <i>from_list</i></code> ] [ <code>-rise_from <i>from_list</i></code> ] [ <code>-fall_from <i>from_list</i></code> ] [ <code>-through <i>through_list</i></code> ] [ <code>-rise_through <i>through_list</i></code> ] [ <code>-fall_through <i>through_list</i></code> ] [ <code>-to <i>to_list</i></code> ] [ <code>-rise_to <i>to_list</i></code> ] [ <code>-fall_to <i>to_list</i></code> ]
<i>group_name</i>	The name of the path group.
<i>weight</i>	Not supported.
<i>range</i>	Not supported.
<i>from_list</i>	A list of clocks, instances, ports or pins.
<i>through_list</i>	A list of instances, pins or nets.
<i>to_list</i>	A list of clocks, instances, ports or pins.

The `group_path` command is used to group paths reported by the `report_checks` command. See `set_false_path` for a description of allowed *from\_list*, *through\_list* and *to\_list* objects.

---

**link** [*cell\_name*]

Alias for `link_design`.

---

**link\_design** [*cell\_name*]

Link (elaborate, flatten) the design with *cell\_name* as the top level cell. The design must be linked after reading netlist and library files. The default value of *cell\_name* is the current design.

The linker creates empty "block box" cells for instances the reference undefined cells when the variable *link\_create\_black\_boxes* is true. When *link\_create\_black\_boxes* is false an error is reported and the link fails.

The `link_design` command returns 1 if the link succeeds and 0 if it fails.

---

<b>make_instance</b>	<i>inst_names</i> <i>lib_cell_name</i>
<i>inst_names</i>	A list of instance names.
<i>lib_cell_name</i>	The library cell of the new instances.

The `make_instance` command makes instances of library cell *lib\_cell\_name*.

---

<b>make_net</b>	<i>net_name_list</i>
<i>net_name_list</i>	A list of net names.

Creates a net for each hierarchical net name.

---

<b>read_liberty</b>	<i>[-corner corner_name]</i> <i>[-min]</i> <i>[-max]</i> <i>[-no_latch_infer]</i> <i>filename</i>
<i>corner_name</i>	Use library for process corner <i>corner_name</i> delay calculation.
<i>-min</i>	Use library for min delay calculation.
<i>-max</i>	Use library for max delay calculation.
<i>filename</i>	The name of the liberty library file to read.

The `read_liberty` command reads a Liberty format library file. The first library that is read sets the units used by SDC/TCL commands and reporting. The `include_file` attribute is supported.

Cells that have a triad of timing arcs between three pins as shown below are inferred as latches:

```

cell (inferred_latch) {
    pin(D) {
        direction : input ;
        timing () {
            related_pin : "E" ;
            timing_type : setup_falling ;
        }
        timing () {
            related_pin : "E" ;
            timing_type : hold_falling ;
        }
    }
    pin(E) {
        direction : input;
    }
    pin(Q) {
        direction : output ;
        timing () {
            related_pin : "D" ;
        }
        timing () {
            related_pin : "E" ;
            timing_type : rising_edge ;
        }
    }
}

```

In this example a positive level-sensitive latch is inferred.

When the `read_liberty -no_latch_infer` flag is used latches are not inferred. If a cell has the `interface_timing true` attribute, no latches are inferred in the cell.

---

<b>read_sdc</b>	[-echo] <i>filename</i>
<b>-echo</b>	Print each command before evaluating its SDC command file.
<b><i>filename</i></b>	SDC command file.

Read SDC commands from *filename*.

The `read_sdc` command stops and reports any errors encountered while reading a file unless `sta_continue_on_error` is 1.

---

<b>read_sdf</b>	[-analysis_type single bc_wc on_chip_variation] [-corner <i>corner_name</i> ] [-type sdf_min sdf_typ sdf_max] [-min_type sdf_min sdf_typ sdf_max] [-max_type sdf_min sdf_typ sdf_max] [-unespaced_dividers] <i>filename</i>
-----------------	---

<code>-analysis_type</code>	See <code>set_operating_conditions</code> for a description of the analysis types.
<code>corner_name</code>	Process corner delays to annotate.
<code>-type</code>	Which of the three values in the SDF tuples to read for analysis type single.
<code>-min_type</code>	Which of the three values in the SDF tuples to read for min paths for analysis type bc_wc or on_chip_variation.
<code>-max_type</code>	Which of the three values in the SDF tuples to read for max paths for analysis type bc_wc or on_chip_variation.
<code>-unescape_dividers</code>	With this option path names in the SDF do not have to escape hierarchy dividers when the path name is escaped. For example, the escaped Verilog name "\inst1/inst2" can be referenced as "inst1/inst2". The correct SDF name is "inst1\inst2", since the divider does not represent a change in hierarchy in this case.
<code>filename</code>	The name of the SDF file to read.

Files compressed with gzip are automatically uncompressed. Compression can reduce the file to less than 10% of its original size.

`INCREMENT` is supported as an alias for `INCREMENTAL`.

The following SDF statements are not supported.

```
PART
INSTANCE wildcards
```

---

<b>read_spef</b>	<ul style="list-style-type: none"> <li>[-min]</li> <li>[-max]</li> <li>[-elmore]</li> <li>[-path <i>path</i>]</li> <li>[-analysis_point <i>ap</i>]</li> <li>[-increment]</li> <li>[-keep_capacitive_coupling]</li> <li>[-coupling_reduction_factor <i>factor</i>]</li> <li>[-reduce_to pi_elmore pi_pole_residue2]</li> <li>[-delete_after_reduce]</li> <li>[-quiet]</li> <li>[-save]</li> </ul> <p><i>filenames</i></p>
<b>-elmore</b>	Ignored (for compatibility purposes only).
<b><i>ap</i></b>	<p>The name of a parasitics analysis point.</p> <p>min - annotate parasitics for min paths.</p> <p>max - annotate parasitics for max paths.</p> <p>min_max - annotate parasitics for min and max paths.</p> <p>The default value is min_max.</p>
<b><i>path</i></b>	Hierarchical instance path to annotate with parasitics.
<b>-increment</b>	Incrementally annotate parasitics (do not remove existing parasitics on annotated nets).
<b>-keep_capacitive_coupling</b>	Keep coupling capacitors in parasitic networks rather than converting them to grounded capacitors.
<b><i>factor</i></b>	Factor to multiply coupling capacitance by when reducing parasitic networks.
<b>-reduce_to</b>	Reduce detailed parasitics to a PI/Elmore or PI/Pole residue model as each net is read.
<b>-delete_after_reduce</b>	Delete the detailed parasitic network after reducing it.
<b>-quiet</b>	Do not print error or warning messages.
<b>-save</b>	Save the parasitics database after reading it (OpenAccess only).

---

<i>filename</i>	The name of the parasitics file to read.
-----------------	--

The `read_spef` command reads a file of net parasitics in SPEF format.

Files compressed with gzip are automatically uncompressed. Compression can reduce the file to less than 10% of its original size.

Separate parasitics can be annotated for min and max paths using the `-min` and `-max` arguments.

With the `-reduce_to` and `-delete_after_reduce` options, parasitic networks are reduced after each net is read, substantially reducing the memory footprint required to store the parasitics.

Coupling capacitors are multiplied by the `-coupling_reduction_factor` when a parasitic network is reduced.

The following SPEF constructs are ignored.

```
*DESIGN_FLOW (all values are ignored)
*S slews
*D driving cell
*I pin capacitances (library cell capacitances are used instead)
*Q r_net load poles
*K r_net load residues
```

If the SPEF file contains triplet values the first value is used.

---

<code>read_verilog</code>	<i>filename</i>
<i>filename</i>	The name of the verilog file to read.

The `read_verilog` command reads a gate level verilog netlist. After all verilog netlist and Liberty libraries are read the design must be linked with the `link_design` command. *filename* can be compressed with gzip.

Verilog 2001 module port declaratation support has been added. An example is shown below.

```
module top (input in1, in2, clk1, clk2, clk3,
            output out);
```

---

<code>replace_cell</code>	<i>instance_list</i>
	<i>replacement_cell</i>
<i>instance_list</i>	A list of instances to swap the cell.
<i>replacement_cell</i>	The replacement lib cell.

The `replace_cell` command changes the cell of an instance. The replacement cell must have the same port list (number, name, and order) as the instance's existing cell for the replacement to be successful.

---

<b>report_annotated_check</b>	[-setup] [-hold] [-recovery] [-removal] [-nochange] [-width] [-period] [-max_skew] [-max_line <i>lines</i> ] [-list_annotated] [-list_not_annotated] [-constant_arcs]
-setup	Report annotated setup checks.
-hold	Report annotated hold checks.
-recovery	Report annotated recovery checks.
-removal	Report annotated removal checks.
-nochange	Report annotated nochange checks.
-width	Report annotated width checks.
-period	Report annotated period checks.
-max_skew	Report annotated max skew checks.
<i>lines</i>	Maximum number of lines listed by the -list_annotated and -list_not_annotated options.
-list_annotated	List annotated timing arcs.
-list_not_annotated	List unannotated timing arcs.
-constant_arcs	Report separate annotation counts for arcs disabled by logic constants (set_logic_one, set_logic_zero).

The `report_annotated_check` command reports a summary of SDF timing check annotation. The `-list_annotated` and `-list_not_annotated` options can be used to list arcs that are annotated or not annotated.

---

<b>report_annotated_delay</b>	[-cell] [-net] [-from_in_ports] [-to_out_ports] [-max_line <i>lines</i> ] [-list_annotated] [-list_not_annotated] [-constant_arcs]
-------------------------------	---

<code>-cell</code>	Report annotated cell delays.
<code>-net</code>	Report annotated internal net delays.
<code>-from_in_ports</code>	Report annotated delays from input ports.
<code>-to_out_ports</code>	Report annotated delays to output ports.
<code>lines</code>	Maximum number of lines listed by the <code>-list_annotated</code> and <code>-list_not_annotated</code> options.
<code>-list_annotated</code>	List annotated timing arcs.
<code>-list_not_annotated</code>	List unannotated timing arcs.
<code>-constant_arcs</code>	Report separate annotation counts for arcs disabled by logic constants ( <code>set_logic_one</code> , <code>set_logic_zero</code> ).

The `report_annotated_delay` command reports a summary of SDF delay annotation. Without the `-from_in_ports` and `-to_out_ports` options annotation of arcs to and from top level ports is not reported. The `-list_annotated` and `-list_not_annotated` options can be used to list arcs that are annotated or not annotated.

---

<code>report_cell</code>	<code>[-connections]</code> <code>[-verbose]</code> <code>instance_path</code> <code>[&gt; filename]</code> <code>[&gt;&gt; filename]</code>
<code>-connections</code>	Report the instance pins.
<code>-verbose</code>	With <code>-connections</code> also report all pins connected to each instance pin net.
<code>instance_path</code>	Hierarchical path to the instance.

The `report_cell` command is an alias for `report_instance`.

---

<b>report_checks</b>	<ul style="list-style-type: none"> <li>[-from <i>from_list</i> <ul style="list-style-type: none"> <li> -rise_from <i>from_list</i></li> <li> -fall_from <i>from_list</i></li> </ul> </li> <li>[-through <i>through_list</i> <ul style="list-style-type: none"> <li> -rise_through <i>through_list</i></li> <li> -fall_through <i>through_list</i></li> </ul> </li> <li>[-to <i>to_list</i> <ul style="list-style-type: none"> <li> -rise_to <i>to_list</i></li> <li> -fall_to <i>to_list</i></li> </ul> </li> <li>[-unconstrained]</li> <li>[-path_delay min min_rise min_fall <ul style="list-style-type: none"> <li> max max_rise max_fall</li> <li> min_max</li> </ul> ]</li> <li>[-group_count <i>path_count</i>]</li> <li>[-endpoint_count <i>endpoint_path_count</i>]</li> <li>[-unique_paths_to_endpoint]</li> <li>[-corner <i>corner_name</i>]</li> <li>[-slack_max <i>max_slack</i>]</li> <li>[-slack_min <i>min_slack</i>]</li> <li>[-sort_by_slack]</li> <li>[-path_group <i>group_names</i>]</li> <li>[-format end full short summary <ul style="list-style-type: none"> <li> full_clock full_clock_expanded</li> </ul> ]</li> <li>[-fields <i>fields</i>]</li> <li>[-digits <i>digits</i>]</li> <li>[-no_line_split]</li> <li>[&gt; <i>filename</i>]</li> <li>[&gt;&gt; <i>filename</i>]</li> </ul>
<i>from_list</i>	A list of clocks, instances, ports or pins.
<i>through_list</i>	A list of instances, pins or nets.
<i>to_list</i>	A list of clocks, instances, ports or pins.
-unconstrained	Report unconstrained paths.
-path_delay min	Report min path (hold) checks.
-path_delay min_rise	Report min path (hold) checks for rising endpoints.
-path_delay min_fall	Report min path (hold) checks for falling endpoints.
-path_delay max	Report max path (setup) checks.

<code>-path_delay max_rise</code>	Report max path (setup) checks for rising endpoints.
<code>-path_delay max_fall</code>	Report max path (setup) checks for falling endpoints.
<code>-path_delay min_max</code>	Report max and max path (setup and hold) checks.
<code>path_count</code>	The number of paths to report in each path group.
<code>endpoint_path_count</code>	The number of paths to report for each endpoint.
<code>-unique_paths_to_endpoint</code>	Report multiple paths to an endpoint that traverse different pins without showing multiple paths with different rise/fall transitions.
<code>corner_name</code>	Only report paths for one process corner.
<code>max_slack</code>	Only report paths with less slack than <code>max_slack</code> .
<code>min_slack</code>	Only report paths with more slack than <code>min_slack</code> .
<code>-sort_by_slack</code>	Sort paths by slack rather than slack grouped by path group.
<code>group_names</code>	List of path group names to report. All path groups are reported if this option is not specified.
<code>-format end</code>	Report path ends with delay, required time and slack.
<code>-format full</code>	Report path start and end points and the path. This is the default path type.
<code>-format full_clock</code>	Report path start and end points, the path, and the source and target clock paths.
<code>-format full_clock_expanded</code>	Report path start and end points, the path, and the source and target clock paths. If the clock is generated and propagated, the path from the clock source pin is also reported.
<code>-format short</code>	Report path start and end points.
<code>-format summary</code>	Report path ends and delay.
<code>fields</code>	List of capacitance transition_time input_pins nets fanout
<code>digits</code>	The number of digits after the decimal point to report. The default value is the variable <code>default_significant_digits</code> .

`-no_line_splits` Do not split long lines into multiple lines.

The `report_checks` command reports paths in the design. See `set_false_path` for a description of allowed `from_list`, `through_list` and `to_list` objects.

Use the `-corner` keyword to report timing for one process corner. With no `-corner` keyword report timing reports the corner with the smallest slack for each timing check.

---

**report\_clock\_properties** `[clock_names]`

`clock_names` List of clock names to report.

The `report_clock_properties` command reports the period and rise/fall edge times for each clock that has been defined.

---

**report\_clock\_skew** `[-setup|-hold]  
[-clock clocks]  
[-digits digits]`

`-setup` Report skew for setup checks.

`-hold` Report skew for hold checks.

`clocks` The target clocks to report.

`digits` The number of digits to report for delays.

Report the clock skew between the source and target clocks for setup or hold timing checks.

---

<b>report_check_types</b>	<code>[-all_violators] [-verbose] [-format slack_only end] [-max_delay] [-min_delay] [-recovery] [-removal] [-clock_gating_setup] [-clock_gating_hold] [-max_transition] [-min_transition] [-min_pulse_width] [-min_period] [-digits digits] [-no_split_lines] [&gt; <i>filename</i>] [&gt;&gt; <i>filename</i>]</code>
<b>-all_violators</b>	All violated timing and design rule constraints are reported.
<b>-verbose</b>	Use a verbose output format.
<b>-format</b>	slack_only reports the minimum slack for each check. end reports the endpoint for each check.
<b>-max_delay</b>	Report setup and max delay path delay constraints.
<b>-min_delay</b>	Report hold and min delay path delay constraints.
<b>-recovery</b>	Report asynchronous recovery checks.
<b>-removal</b>	Report asynchronous removal checks.
<b>-clock_gating_setup</b>	Report gated clock enable setup checks.
<b>-clock_gating_hold</b>	Report gated clock hold setup checks.
<b>-max_transition</b>	Report max transition design rule checks.
<b>-max_skew</b>	Report max skew design rule checks.
<b>-min_pulse_width</b>	Report min pulse width design rule checks.

<code>-min_period</code>	Report min period design rule checks.
<code>-min_transition</code>	Report min transition design rule checks.
<code>digits</code>	The number of digits after the decimal point to report. The default is <code>default_significant_digits</code> .
<code>-no_split_lines</code>	

The `report_check_types` command reports the slack for each type of timing and design rule constraint. The keyword options allow a subset of the constraint types to be reported.

---

<code>report_dcabc</code>	<code>[-from <i>from_pin</i>] [-to <i>to_pin</i>] [-corner <i>corner_name</i>] [-min] [-max] [-digits <i>digits</i>] [&gt; <i>filename</i>] [&gt;&gt; <i>filename</i>]</code>
<code><i>from_pin</i></code>	An instance pin.
<code><i>to_pin</i></code>	An instance pin.
<code><i>digits</i></code>	The number of digits after the decimal point to report. The default is <code>default_significant_digits</code> .

The `report_dcabc` command shows how the delays between instance pins are calculated. It is useful for debugging problems with delay calculation.

Use the `-corner` keyword to specify a process corner. The `-corner` keyword is required if more than one process corner is defined.

---

#### `report_disabled_edges`

The `report_disabled_edges` command reports disabled timing arcs along with the reason they are disabled. Each disabled timing arc is reported as the instance name along with the from and to ports of the arc. The disable reason is shown next. Arcs that are disabled with `set_disable_timing` are reported with `constraint` as the reason. Arcs that are disabled by constants are reported with `constant` as the reason along with the constant instance pin and value. Arcs that are disabled to break combinational feedback loops are reported with `loop` as the reason.

```
> report_disable_timing
u1 A B constant B=0
```

---

<b>report_instance</b>	<code>[-connections] [-verbose] <i>instance_path</i> [&gt; <i>filename</i>] [&gt;&gt; <i>filename</i>]</code>
<code>-connections</code>	Report the pins connected to the net.
<code>-verbose</code>	Report the capacitance of each pin.
<code><i>instance_path</i></code>	Hierarchical path to a instance.

---

<b>report_lib_cell</b>	<code><i>cell_name</i> [&gt; <i>filename</i>] [&gt;&gt; <i>filename</i>]</code>
<code><i>cell_name</i></code>	The name of a library cell.

Describe the liberty library cell `cell_name`.

---

<b>report_net</b>	<code>[-connections] [-verbose] [-significant_digits <i>digits</i>] <i>net_path</i> [&gt; <i>filename</i>] [&gt;&gt; <i>filename</i>]</code>
<code>-connections</code>	Report the net pins.
<code>-verbose</code>	With <code>-connections</code> also report all pins connected to each instance pin net.
<code><i>net_path</i></code>	Hierarchical path to a net.

---

<b>report_pin</b>	<code><i>pin_path</i> [&gt; <i>filename</i>] [&gt;&gt; <i>filename</i>]</code>
-------------------	--

---

*pin\_path* Hierarchical path to a pin.

---

**report\_power** [-instance *instance*]  
[-digits *digits*]  
[> *filename*]  
[>> *filename*]

*instance* Report the power for *instance*.

*digits* The number of digits after the decimal point to report. The default is `default_significant_digits`.

Report power used by the design or a specific instance. The internal, switching, leakage and total power are reported. Design power is reported separately for combinational, sequential, macro and pad groups.

---

**report\_pulse\_width\_checks** [-verbose]  
[-digits *digits*]  
[-no\_line\_splits]  
[*pins*]  
[> *filename*]  
[>> *filename*]

**-verbose** Use a verbose output format.

*digits* The number of digits after the decimal point to report. The default is `default_significant_digits`.

**-no\_line\_splits**

*pins* List of pins or ports to report.

The `report_pulse_width_checks` command reports min pulse width checks for pins in the clock network. If *pins* is not specified all clock network pins are reported.

---

<b>set_assigned_check</b>	<code>-setup -hold -recovery -removal [-rise] [-fall] [-corner <i>corner_name</i>] [-min] [-max] [-from <i>from_pins</i>] [-to <i>to_pins</i>] [-clock rise fall] [-cond sdf_cond] [-worst] <i>margin</i></code>
<code>-setup -hold -recovery -removal</code>	The timing check type to annotate.
<code>-rise</code>	Annotate the rising delays.
<code>-fall</code>	Annotate the falling delays.
<code><i>corner_name</i></code>	The name of a process corner.
<code>-min</code>	Annotate the minimum value of the process corner.
<code>-max</code>	Annotate the maximum value of the process corner.
<code><i>from_pins</i></code>	A list of pins for the clock.
<code><i>to_pins</i></code>	A list of pins for the data.
<code>-clock</code>	The clock pin transition.
<code>-worst</code>	Ignored.
<code><i>margin</i></code>	The timing check value.

The `set_assigned_check` command is used to annotate the timing checks between two pins on an instance. The annotated delay overrides the calculated delay. This command is a interactive way to back-annotate delays like an SDF file.

Use the `-corner` keyword to specify a process corner. The `-corner` keyword is required if more than one process corner is defined.

---

<b>set_assigned_delay</b>	<code>-cell -net [-rise] [-fall] [-corner <i>corner_name</i>] [-min] [-max] [-from <i>from_pins</i>] [-to <i>to_pins</i>] <i>delay</i></code>
<code>-cell</code>	Annotate the delays between two pins on an instance.
<code>-net</code>	Annotate the delays between two pins on a net.
<code>-rise</code>	Annotate the rising delays.
<code>-fall</code>	Annotate the falling delays.
<code>-min</code>	Annotate the minimum delays.
<code>-max</code>	Annotate the maximum delays.
<code><i>from_pins</i></code>	A list of pins.
<code><i>to_pins</i></code>	A list of pins.
<code><i>delay</i></code>	The delay between <code><i>from_pins</i></code> and <code><i>to_pins</i></code> .

The `set_assigned_delay` command is used to annotate the delays between two pins on an instance or net. The annotated delay overrides the calculated delay. This command is a interactive way to back-annotate delays like an SDF file.

Use the `-corner` keyword to specify a process corner. The `-corner` keyword is required if more than one process corner is defined.

---

<b>set_assigned_transition</b>	<code>[-rise] [-fall] [-corner <i>corner_name</i>] [-min] [-max] <i>slew</i> <i>pin_list</i></code>
<code>-rise</code>	Annotate the rising transition.

<code>-fall</code>	Annotate the falling transition.
<code>-min</code>	Annotate the minimum transition time.
<code>-max</code>	Annotate the maximum transition time.
<code>slew</code>	The pin transition time.
<code>pin_list</code>	A list of pins.

The `set_assigned_transition` command is used to annotate the transition time (slew) of a pin. The annotated transition time overrides the calculated transition time.

Use the `-corner` keyword to specify a process corner. The `-corner` keyword is required if more than one process corner is defined.

---

<code>set_case_analysis</code>	<code>0 1 zero one rise rising fall falling</code> <code>port_or_pin_list</code>
<code>port_or_pin_list</code>	A list of ports or pins.

The `set_case_analysis` command sets the signal on a port or pin to a constant logic value. No paths are propagated from constant pins. Constant values set with the `set_case_analysis` command are propagated through downstream gates in all modes (unlike `set_logic_zero`, etc).

---

<code>set_clock_gating_check</code>	<code>[-setup setup_time]</code> <code>[-hold hold_time]</code> <code>[-rise]</code> <code>[-fall]</code> <code>[-high]</code> <code>[-low]</code> <code>[objects]</code>
<code>setup_time</code>	Clock enable setup margin.
<code>hold_time</code>	Clock enable hold margin.
<code>-rise</code>	The setup/hold margin is for the rising edge of the clock enable.
<code>-fall</code>	The setup/hold margin is for the falling edge of the clock enable.

**-high** The gating clock is active high (pin and instance objects only).

**-low** The gating clock is active low (pin and instance objects only).

**objects** A list of clocks, instances, pins or ports.

The `set_clock_gating_check` command is used to add setup or hold timing checks for data signals used to gate clocks.

If no objects are specified the setup/hold margin is global and applies to all clock gating circuits in the design. If neither of the `-rise` and `-fall` options are used the setup/hold margin applies to the rising and falling edges of the clock gating signal.

Normally the library cell function is used to determine the active state of the clock. The clock is active high for AND/NAND functions and active low for OR/NOR functions. The `-high` and `-low` options are used to specify the active state of the clock for other cells, such as a MUX.

If multiple `set_clock_gating_check` commands apply to a clock gating instance the priority of the commands is shown below (highest to lowest priority).

clock enable pin  
instance  
clock pin  
clock  
global

---

**set\_clock\_groups** [-name *name*]  
[-logically\_exclusive]  
[-physically\_exclusive]  
[-asynchronous]  
[-allow\_paths]  
-group *clocks*

---

**name** The clock group name.

---

**-logically\_exclusive** The clocks in different groups do not interact logically but can be physically present on the same chip. Paths between clock groups are considered for noise analysis.

---

**-physically\_exclusive** The clocks in different groups cannot be present at the same time on a chip. Paths between clock groups are not considered for noise analysis.

---

**-asynchronous** The clock groups are asynchronous. Paths between clock groups are considered for noise analysis.

---

```
-allow_paths
```

```
clocks
```

 A list of clocks in the group.

The `set_clock_groups` command is used to define groups of clocks that interact with each other. Clocks in different groups do not interact and paths between them are not reported. Use a `-group` argument for each clock group.

---

```
set_clock_latency
```

 [-source]  
[-clock *clock*]  
[-rise]  
[-fall]  
[-min]  
[-max]  
*delay*  
*objects*

```
-source
```

 The latency is at the clock source.

```
clock
```

 If multiple clocks are defined at a pin this use this option to specify the latency for a specific clock.

```
-rise
```

 The latency is for the rising edge of the clock.

```
-fall
```

 The latency is for the falling edge of the clock.

```
-min
```

*delay* is the minimum latency.

```
-max
```

*delay* is the maximum latency.

```
delay
```

 Clock source or insertion delay.

```
objects
```

 A list of clocks, pins or ports.

The `set_clock_latency` command describes expected delays of the clock tree when analyzing a design using ideal clocks. Use the `-source` option to specify latency at the clock source, also known as insertion delay. Source latency is delay in the clock tree that is external to the design or a clock tree internal to an instance that implements a complex logic function.

---

```
set_clock_sense
```

 [-positive]  
[-negative]  
[-pulse *pulse\_type*]  
[-stop\_propagation]  
[-clock *clocks*]  
*pins*

---

<code>-positive</code>	The clock sense is positive unite.
<code>-negative</code>	The clock sense is negative unite.
<code>pulse_type</code>	<code>rise_triggered_high_pulse</code> <code>rise_triggered_low_pulse</code> <code>fall_triggered_high_pulse</code> <code>fall_triggered_low_pulse</code>
<code>-stop_propagation</code>	Stop propagating <code>clocks</code> clocks at <code>pins</code> .
<code>clocks</code>	A list of <code>clocks</code> to apply the sense
<code>pins</code>	A list of pins.

---

The `set_clock_sense` command is used to modify the propagation of a clock signal. The clock sense is set with the `-positive` and `-negative` flags. Use the `-stop_propagation` flag to stop the clock from propagating beyond a pin. The `-positive`, `-negative`, `-stop_propagation`, and `-pulse` options are mutually exclusive. If the `-clock` option is not used the command applies to all clocks that traverse `pins`. The `-pulse` option is currently not supported.

---

<code>set_clock_transition</code>	<code>[-rise]</code> <code>[-fall]</code> <code>[-min]</code> <code>[-max]</code> <code>transition</code> <code>clocks</code>
<code>-rise</code>	The transition time is for the rising edge of the clock.
<code>-fall</code>	The transition time is for the falling edge of the clock.
<code>-min</code>	<code>transition</code> is the minimum transition time.
<code>-max</code>	<code>transition</code> is the maximum transition time.
<code>transition</code>	Clock transition time (slew).
<code>clocks</code>	A list of <code>clocks</code> .

---

The `set_clock_transition` command describes expected transition times of the clock tree when analyzing a design using ideal clocks.

---

<b>set_clock_uncertainty</b>	<code>[-from -rise_from -fall_from <i>from_clock</i>]  <code>[-to -rise_to -fall_to <i>to_clock</i>]  <code>[-rise]  <code>[-fall]  <code>[-setup]  <code>[-hold]  <code><i>uncertainty</i>  <code>[<i>objects</i>]</code> </code></code></code></code></code></code></code>
<i>from_clock</i>	
<i>to_clock</i>	
<code>-rise</code>	The uncertainty is for the rising edge of the clock.
<code>-fall</code>	The uncertainty is for the falling edge of the clock.
<code>-setup</code>	<i>uncertainty</i> is the setup check uncertainty.
<code>-hold</code>	<i>uncertainty</i> is the hold uncertainty.
<i>uncertainty</i>	Clock uncertainty.
<i>objects</i>	A list of clocks, ports or pins.

The `set_clock_uncertainty` command specifies the uncertainty or jitter in a clock.

---

<b>set_data_check</b>	<code>[-from <i>from_object</i>]  <code>[-rise_from <i>from_object</i>]  <code>[-fall_from <i>from_object</i>]  <code>[-to <i>to_object</i>]  <code>[-rise_to <i>to_object</i>]  <code>[-fall_to <i>to_object</i>]  <code>[-setup]  <code>[-hold]  <code>[-clock <i>clock</i>]  <code><i>margin</i></code> </code></code></code></code></code></code></code></code></code>
<i>from_object</i>	A pin used as the timing check reference.
<i>to_object</i>	A pin that the setup/hold check is applied to.
<code>-setup</code>	Add a setup timing check.

<code>-hold</code>	Add a hold timing check.
<code>clock</code>	The setup/hold check clock.
<code>margin</code>	The setup or hold time margin.

The `set_data_check` command is used to add a setup or hold timing check between two pins.

---

**`set_disable_inferred_clock_gating`**

<code>objects</code>	A list of clock gating instances, clock gating pins, or clock enable pins.
----------------------	--

The `set_disable_inferred_clock_gating` command disables clock gating checks on a clock gating instance, clock gating pin, or clock gating enable pin.

---

**`set_disable_timing`**      `[-from from_port]`  
`[-to to_port]`  
`objects`

`from_port`

`to_port`

<code><i>objects</i></code>	A list of instances, ports, pins, cells or [library/]cell/port.
-----------------------------	---

The `set_disable_timing` command is used to disable paths through pins in the design. There are many different forms of the command depending on the objects specified in `objects`.

All timing paths through an instance are disabled when `objects` contains an instance. Timing checks in the instance are *not* disabled.

```
set_disable_timing u2
```

The `-from` and `-to` options can be used to restrict the disabled path to those from, to or between specific pins on the instance.

```
set_disable_timing -from A u2
set_disable_timing -to Z u2
set_disable_timing -from A -to Z u2
```

A list of top level ports or instance pins can also be disabled.

```
set_disable_timing u2/Z
set_disable_timing in1
```

Timing paths through all instances of a library cell in the design can be disabled by naming the cell using a hierarchy separator between the library and cell name. Paths from or to a cell port can be disabled with the `-from` and `-to` options or a port name after library and cell names.

```
set_disable_timing liberty1/snl_bufx2
set_disable_timing -from A liberty1/snl_bufx
set_disable_timing -to Z liberty1/snl_bufx
set_disable_timing liberty1/snl_bufx2/A
```

---

<b>set_drive</b>	<code>[-rise]</code> <code>[-fall]</code> <code>[-max]</code> <code>[-min]</code> <i>resistance</i> <i>port_list</i>
------------------	---

`-rise` This is the drive resistance of the rising edge of the input.

`-fall` This is the drive resistance of the falling edge of the input.

`-max` This is the drive resistance for maximum path delays.

`-min` This is the drive resistance for minimum path delays.

*resistance* The external drive resistance.

*port\_list* A list of ports.

The `set_drive` command describes the resistance of an input port external driver.

---

<b>set_driving_cell</b>	<code>[-lib_cell <i>cell_name</i>]</code> <code>[-library <i>library</i>]</code> <code>[-rise]</code> <code>[-fall]</code> <code>[-min]</code> <code>[-max]</code> <code>[-pin <i>pin</i>]</code> <code>[-from_pin <i>from_pin</i>]</code> <code>[-input_transition_rise <i>trans_rise</i>]</code> <code>[-input_transition_fall <i>trans_fall</i>]</code> <i>port_list</i>
-------------------------	---

*cell\_name* The cell of driver.

<i>library</i>	The library of the driving cell.
<i>-rise</i>	This is the driving cell for the rising edge of the input.
<i>-fall</i>	This is the driving cell for the falling edge of the input.
<i>-max</i>	This is the driving cell for maximum path delays.
<i>-min</i>	This is the driving cell for minimum path delays.
<i>pin</i>	The output port of the driving cell.
<i>from_pin</i>	Use paths through the driving cell from this pin to the output pin.
<i>trans_rise</i>	The transition time for a rising input at <i>from_pin</i> .
<i>trans_fall</i>	The transition time for a falling input at <i>from_pin</i> .
<i>port_list</i>	A list of ports.

The `set_driving_cell` command describes an input port external driver.

---

<b>set_false_path</b>	<ul style="list-style-type: none"> <li>[-setup]</li> <li>[-hold]</li> <li>[-rise]</li> <li>[-fall]</li> <li>[-from <i>from_list</i>]</li> <li>[-rise_from <i>from_list</i>]</li> <li>[-fall_from <i>from_list</i>]</li> <li>[-through <i>through_list</i>]</li> <li>[-rise_through <i>through_list</i>]</li> <li>[-fall_through <i>through_list</i>]</li> <li>[-to <i>to_list</i>]</li> <li>[-rise_to <i>to_list</i>]</li> <li>[-fall_to <i>to_list</i>]</li> <li>[-reset_path]</li> </ul>
<i>-setup</i>	Only apply to setup checks.
<i>-hold</i>	Only apply to hold checks.

<code>-rise</code>	Only apply to rising path edges.
<code>-fall</code>	Only apply to falling path edges.
<code>-reset_path</code>	Remove any matching <code>set_false_path</code> , <code>set_multicycle_path</code> , <code>set_max_delay</code> , <code>set_min_delay</code> exceptions first.
<code>from_list</code>	A list of clocks, instances, ports or pins.
<code>through_list</code>	A list of instances, pins or nets.
<code>to_list</code>	A list of clocks, instances, ports or pins.

The `set_false_path` command disables timing along a path from, through and to a group of design objects.

Objects in `from_list` can be clocks, register/latch instances, or register/latch clock pins. The `-rise_from` and `-fall_from` keywords restrict the false paths to a specific clock edge.

Objects in `through_list` can be nets, instances, instance pins, or hierarchical pins,. The `-rise_through` and `-fall_through` keywords restrict the false paths to a specific path edge that traverses through the object.

Objects in `to_list` can be clocks, register/latch instances, or register/latch clock pins. The `-rise_to` and `-fall_to` keywords restrict the false paths to a specific transition at the path end.

---

<code>set_fanout_load</code>	<i>fanout</i>
	<i>port_list</i>

This command is ignored.

---

<code>set_hierarchy_separator</code>	<i>separator</i>
<i>separator</i>	Character used to separate hierarchical names.

Set the character used to separate names in a hierarchical instance, net or pin name. This separator is used by the command interpreter to read arguments and print results. The default separator is '/'.

---

<code>set_ideal_latency</code>	<code>[-rise] [-fall] [-min] [-max] delay objects</code>
--------------------------------	--

The `set_ideal_latency` command is parsed but ignored.

---

<code>set_ideal_network</code>	<code>[-no_propagation] objects</code>
--------------------------------	--

The `set_ideal_network` command is parsed but ignored.

---

```
set_ideal_transition      [-rise] [-fall] [-min] [-max] transition_time
                           objects
```

The `set_ideal_transition` command is parsed but ignored.

---

<code>set_input_delay</code>	<code>[-rise] [-fall] [-max] [-min] [-clock <i>clock</i>] [-clock_fall] [-reference_pin <i>ref_pin</i>] [-source_latency_included] [-network_latency_included] [-add_delay] <i>delay</i> <i>port_pin_list</i></code>
<code>-rise</code>	This is the arrival time for the rising edge of the input.
<code>-fall</code>	This is the arrival time for the falling edge of the input.
<code>-max</code>	This is the minimum arrival time.
<code>-min</code>	This is the maximum arrival time.
<code><i>clock</i></code>	The arrival time is from this <code>clock</code> .
<code>-clock_fall</code>	The arrival time is from the falling edge of <code>clock</code>
<code><i>ref_pin</i></code>	The arrival time is with respect to the <code>clock</code> that arrives at <code>ref_pin</code> .
<code>-source_latency_included</code>	If <code>-source_latency_included</code> is not specified the <code>clock</code> source latency (insertion delay) is added to the delay value.
<code>-network_latency_included</code>	If <code>-network_latency_included</code> is not specified and the <code>clock</code> is ideal the <code>clock</code> latency is added to the delay value.

**-add\_delay** Add this arrival to any existing arrivals on *port\_pin\_list*.

**delay** The arrival time after *clock*.

**pin\_port\_list** A list of pins or ports.

The `set_input_delay` command is used to specify the arrival time of an input signal. Unless the `-add_delay` option is specified, any existing arrival time is replaced.

The `-reference_pin` option is used to specify an arrival time with respect to the arrival on a pin in the clock network. For propagated clocks, the input arrival time is relative to the clock arrival time at the reference pin (the clock source latency and network latency from the clock source to the reference pin). For ideal clocks, input arrival time is relative to the reference pin clock source latency. With the `-clock_fall` flag the arrival time is relative to the falling transition at the reference pin. If no clocks arrive at the reference pin the `set_input_delay` command is ignored. If no `-clock` is specified the arrival time is with respect to all clocks that arrive at the reference pin. The `-source_latency_included` and `-network_latency_included` options cannot be used with `-reference_pin`.

---

**set\_input\_transition** [-rise]  
[-fall]  
[-max]  
[-min]  
*transition*  
*port\_list*

**-rise** This is the transition time for the rising edge of the input.

**-fall** This is the transition time for the falling edge of the input.

**-max** This is the minimum transition time.

**-min** This is the maximum transition time.

***transition*** The transition time (slew).

***port\_list*** A list of ports.

The `set_input_transition` command is used to specify the transition time (slew) of an input signal.

---

**set\_level\_shifter\_strategy** [-rule *rule\_type*]

This command is parsed and ignored by timing analysis.

---

```
set_level_shifter_threshold [-voltage voltage]
```

This command is parsed and ignored by timing analysis.

---

<b>set_load</b>	[-rise] [-fall] [-max] [-min] [-subtract_pin_load] [-pin_load] [-wire_load] <i>capacitance</i> <i>objects</i>
-rise	The capacitance is for rising edge delays.
-fall	The capacitance is for falling edge delays.
-max	The capacitance is for maximum path delays.
-min	The capacitance is for minimum path delays.
-subtract_pin_load	Subtract the capacitance of all instance pins connected to the net from wire <i>capacitance</i> .
-pin_load	<i>capacitance</i> is external instance pin capacitance (ports only).
-wire_load	<i>capacitance</i> is external wire capacitance (ports only).
<i>capacitance</i>	The capacitance, in library capacitance units.
<i>objects</i>	A list of nets or ports.

The `set_load` command annotates capacitance on a net or port.

Ports can have external wire or pin capacitance that is annotated separately with the `-pin_load` and `-wire_load` options. Without the `-pin_load` and `-wire_load` options pin capacitance is annotated. External capacitances are used by delay calculator to find output driver delays and transition times.

Net wire capacitance can also be annotated with the `set_load` command. If the `-subtract_pin_load` option is specified the capacitance of all instance pins connected to the net is subtracted from *capacitance*.

---

```
set_logic_dc          port_list
```

*port\_pin\_list* List of ports or pins.

Set a port or pin to a constant unknown logic value. No paths are propagated from constant pins.

**set\_logic\_one** *port\_list*

*port\_pin\_list* List of ports or pins.

Set a port or pin to a constant logic one value. No paths are propagated from constant pins.

**set\_logic\_zero** *port\_list*

*port\_pin\_list* List of ports or pins.

Set a port or pin to a constant logic zero value. No paths are propagated from constant pins.

**set\_max\_area** *area*

area

The `set_max_area` command is ignored during timing but is included in SDC files that are written.

**set\_max\_capacitance** *capacitance objects*

*capacitance*

*objects* List of ports or cells.

The `set_max_capacitance` command is ignored during timing but is included in SDC files that are written.

---

<b>set_max_delay</b>	<code>[-rise]  [-fall]  [-from <i>from_list</i>]  [-rise_from <i>from_list</i>]  [-fall_from <i>from_list</i>]  [-through <i>through_list</i>]  [-rise_through <i>through_list</i>]  [-fall_through <i>through_list</i>]  [-to <i>to_list</i>]  [-rise_to <i>to_list</i>]  [-fall_to <i>to_list</i>]  [-reset_path]  [-ignore_clock_latency]  <i>delay</i></code>
<b>-rise</b>	Only constrain paths to rising edges.
<b>-fall</b>	Only constrain paths to falling edges.
<b><i>from_list</i></b>	A list of clocks, instances, ports or pins.
<b><i>through_list</i></b>	A list of instances, pins or nets.
<b><i>to_list</i></b>	A list of clocks, instances, ports or pins.
<b>-ignore_clock_latency</b>	Ignore clock latency at the source and target registers.
<b>-reset_path</b>	Remove any matching <code>set_false_path</code> , <code>set_multicycle_path</code> , <code>set_max_delay</code> , <code>set_min_delay</code> exceptions first.
<b><i>delay</i></b>	The maximum delay.

The `set_max_delay` command constrains the maximum delay through combinational logic paths. See `set_false_path` for a description of allowed *from\_list*, *through\_list* and *to\_list* objects. If the *to\_list* ends at a timing check the setup/hold time is included in the path delay.

When the `-ignore_clock_latency` option is used clock latency at the source and destination of the path delay is ignored. The constraint is reported in the default path group (`**default**`) rather than the clock path group when the path ends at a timing check.

---

<b>set_max_dynamic_power</b>	<i>power [unit]</i>
------------------------------	---------------------

The `set_max_dynamic_power` command is ignored.

---

<b>set_max_fanout</b>	<i>fanout</i> <i>objects</i>
<i>fanout</i>	

*objects* List of ports or cells.

The `set_max_fanout` command is ignored during timing but is included in SDC files that are written.

---

<b>set_max_leakage_power</b>	<i>power</i> [ <i>unit</i> ]
------------------------------	------------------------------

The `set_max_leakage_power` command is ignored.

---

<b>set_max_time_borrow</b>	<i>delay</i> <i>objects</i>
<i>delay</i>	The maximum time the latches can borrow.
<i>objects</i>	List of clocks, instances or pins.

The `set_max_time_borrow` command specifies the maximum amount of time that latches can borrow. Time borrowing is the time that a data input to a transparent latch arrives after the latch opens.

---

<b>set_max_transition</b>	<code>[-data_path]</code> <code>[-clock_path]</code> <code>[-rise]</code> <code>[-fall]</code> <i>transition</i> <i>objects</i>
<i>transition</i>	The maximum transition time (slew).
<i>objects</i>	List of clocks, ports or designs.

The `set_max_transition` command specifies the maximum transition time (slew) design rule checked by the `report_constraint -max_transition` command.

If specified for a design, the default maximum transition is set for the design.

If specified for a clock, the maximum transition is applied to all pins in the clock domain. The `-clock_path` option restricts the maximum transition to clocks in clock paths. The `-data_` input option restricts the maximum transition to clocks data paths. The `-clock_path`, `-data_path`, `-rise` and `-fall` options only apply to clock objects.

---

<b>set_min_capacitance</b>	<i>capacitance objects</i>
<i>capacitance</i>	
<i>objects</i>	List of ports or cells.

The `set_min_capacitance` command is ignored during timing but is included in SDC files that are written.

---

<b>set_min_delay</b>	<code>[-rise] [-fall] [-from <i>from_list</i>] [-rise_from <i>from_list</i>] [-fall_from <i>from_list</i>] [-through <i>through_list</i>] [-rise_through <i>through_list</i>] [-fall_through <i>through_list</i>] [-to <i>to_list</i>] [-rise_to <i>to_list</i>] [-fall_to <i>to_list</i>] [-ignore_clock_latency] [-reset_path] <i>delay</i></code>
<i>-rise</i>	Only constrain paths to rising edges.
<i>-fall</i>	Only constrain paths to falling edges.
<i>from_list</i>	A list of clocks, instances, ports or pins.
<i>through_list</i>	A list of instances, pins or nets.
<i>to_list</i>	A list of clocks, instances, ports or pins.
<i>-ignore_clock_latency</i>	Ignore clock latency at the source and target registers.
<i>-reset_path</i>	Remove any matching <code>set_false_path</code> , <code>set_multicycle_path</code> , <code>set_max_delay</code> , <code>set_min_delay</code> exceptions first.
<i>delay</i>	The minimum delay.

The `set_min_delay` command constrains the minimum delay through combinational logic. See `set_false_path` for a description of allowed *from\_list*, *through\_list* and *to\_list* objects. If the *to\_list* ends at a timing check the setup/hold time is included in the path delay.

When the `-ignore_clock_latency` option is used clock latency at the source and destination of the path delay is ignored. The constraint is reported in the default path group (`**default**`) rather than the clock path group when the path ends at a timing check.

---

<code>set_min_pulse_width</code>	<code>[-high] [-low] <i>min_width</i> <i>objects</i></code>
<code>-high</code>	Set the minimum high pulse width.
<code>-low</code>	Set the minimum low pulse width.
<code><i>min_width</i></code>	
<code><i>objects</i></code>	List of pins, instances or clocks.

If `-low` and `-high` are not specified the minimum width applies to both high and low pulses.

---

<code>set_multicycle_path</code>	<code>[-setup] [-hold] [-rise] [-fall] [-start] [-end] [-from <i>from_list</i>] [-rise_from <i>from_list</i>] [-fall_from <i>from_list</i>] [-through <i>through_list</i>] [-rise_through <i>through_list</i>] [-fall_through <i>through_list</i>] [-to <i>to_list</i>] [-rise_to <i>to_list</i>] [-fall_to <i>to_list</i>] [-reset_path] <i>path_multiplier</i></code>
<code>-setup</code>	Only apply to setup checks.
<code>-hold</code>	Only apply to hold checks.
<code>-rise</code>	Only apply to rising path edges.
<code>-fall</code>	Only apply to falling path edges.

<code>-start</code>	Multiply the source clock period by <i>period_multiplier</i> .
<code>-end</code>	Multiply the target clock period by <i>period_multiplier</i> .
<code>-reset_path</code>	Remove any matching <code>set_false_path</code> , <code>set_multicycle_path</code> , <code>set_max_delay</code> , <code>set_min_delay</code> exceptions first.
<code>from_list</code>	A list of clocks, instances, ports or pins.
<code>through_list</code>	A list of instances, pins or nets.
<code>to_list</code>	A list of clocks, instances, ports or pins.
<code>path_multiplier</code>	The number of clock periods to add to the path required time.

Normally the path between two registers or latches is assumed to take one clock cycle. The `set_multicycle_path` command overrides this assumption and allows multiple clock cycles for a timing check. See `set_false_path` for a description of allowed `from_list`, `through_list` and `to_list` objects.

---

<code>set_operating_conditions</code>	<code>[-analysis_type single bc_wc on_chip_variation]</code> <code>[-library lib]</code> <code>[condition]</code> <code>[-min min_condition]</code> <code>[-max max_condition]</code> <code>[-min_library min_lib]</code> <code>[-max_library max_lib]</code>
<code>single</code>	Use one operating condition for min and max paths.
<code>bc_wc</code>	Best case, worst case analysis. Setup checks use <code>max_condition</code> for clock and data paths. Hold checks use the <code>min_condition</code> for clock and data paths.
<code>on_chip_variation</code>	The min and max operating conditions represent variations on the chip that can occur simultaneously. Setup checks use <code>max_condition</code> for data paths and <code>min_condition</code> for clock paths. Hold checks use <code>min_condition</code> for data paths and <code>max_condition</code> for clock paths. This is the default analysis type.
<code>lib</code>	The name of the library that contains <code>condition</code> .
<code>condition</code>	The operating condition for analysis type <code>single</code> .

<i>min_condition</i>	The operating condition to use for min paths and hold checks.
<i>max_condition</i>	The operating condition to use for max paths and setup checks.
<i>min_lib</i>	The name of the library that contains <i>min_condition</i> .
<i>max_lib</i>	The name of the library that contains <i>max_condition</i> .

The `set_operating_conditions` command is used to specify the type of analysis performed and the operating conditions used to derate library data.

---

<b>set_output_delay</b>	<code>[-rise]</code> <code>[-fall]</code> <code>[-max]</code> <code>[-min]</code> <code>[-clock <i>clock</i>]</code> <code>[-clock_fall]</code> <code>[-reference_pin <i>ref_pin</i>]</code> <code>[-source_latency_included]</code> <code>[-network_latency_included]</code> <code>[-add_delay]</code> <code><i>delay</i></code> <code><i>port_pin_list</i></code>
<code>-rise</code>	This is the arrival time for the rising edge of the input.
<code>-fall</code>	This is the arrival time for the falling edge of the input.
<code>-max</code>	This is the minimum arrival time.
<code>-min</code>	This is the maximum arrival time.
<code><i>clock</i></code>	The departure time is from this clock.
<code>-clock_fall</code>	The departure time is from the falling edge of <code><i>clock</i></code> .
<code><i>ref_pin</i></code>	The departure time is with respect to the clock that arrives at <code><i>ref_pin</i></code> .

**-add\_delay** Add this departure to any existing arrivals on *port\_pin\_list*.

*delay* The departure time after *clock*.

*pin\_port\_list* A list of pins or ports.

The `set_output_delay` command is used to specify the departure time of an output signal. Unless the `-add_delay` option is specified any existing departure time is replaced.

The `-reference_pin` option is used to specify a departure time with respect to the arrival on a pin in the clock network. For propagated clocks, the output departure time is relative to the clock arrival time at the reference pin (the clock source latency and network latency from the clock source to the reference pin). For ideal clocks, output departure time is relative to the reference pin clock source latency. With the `-clock_fall` flag the departure time is relative to the falling transition at the reference pin. If no clocks arrive at the reference pin the `set_output_delay` command is ignored. If no `-clock` is specified the departure time is with respect to all clocks that arrive at the reference pin. The `-source_latency_included` and `-network_latency_included` options cannot be used with `-reference_pin`.

---

**set\_port\_fanout\_number** [-min]  
[-max]  
*fanout*  
*port\_list*

*-min* The fanout for minimum path delay calculation.

*-max* The fanout for maximum path delay calculation.

*fanout* The external fanout of the ports.

*port\_list* A list of ports.

---

**set\_propagated\_clock** *objects*

*objects* A list of clocks, ports or pins.

The `set_propagated_clock` command changes a clock tree from an ideal network that has no delay one that uses calculated or back-annotated gate and interconnect delays. When *objects* is a port or pin, clock delays downstream of the object are used.

---

<b>set_pvt</b>	<i>instances</i> [-min] [-max] [-process <i>process</i> ] [-voltage <i>voltage</i> ] [-temperature <i>temperature</i> ]
<i>instances</i>	A list instances.
-min	Only set the PVT values for max delay paths.
-max	Only set the PVT values for min delay paths.
<i>process</i>	A process value (float).
<i>voltage</i>	A voltage value (float).
<i>temperature</i>	A temperature value (float).

The `set_pvt` command sets the process, voltage and temperature values used during delay calculation for a specific instance in the design.

---

<b>set_timing_derate</b>	[-rise] [-fall] [-early] [-late] [-clock] [-data] [-net_delay] [-cell_delay] [-cell_check] <i>derate</i> [ <i>objects</i> ]
-early	Derate early (min) paths.
-late	Derate late (max) paths.
-clock	Derate paths in the clock network.
-data	Derate data paths.

<code>-net_delay</code>	Derate net (interconnect) delays.
<code>-cell_delay</code>	Derate cell delays.
<code>-cell_check</code>	Derate cell timing check margins.
<code>derate</code>	The derating factor (0.0 to 1.0).
<code>objects</code>	A list of instances, library cells, or nets.

The `set_timing_derate` command is used to derate delay calculation results used by the STA. If the `-early` and `-late` flags are omitted the both min and max paths are derated. If the `-clock` and `-data` flags are not used the derating both clock and data paths are derated.

Use the `reset_timing_derate` command to remove all derating factors.

---

<code>set_resistance</code>	<code>[-max]</code> <code>[-min]</code> <code>resistance</code> <code>net_list</code>
<code>-min</code>	The resistance for minimum path delay calculation.
<code>-max</code>	The resistance for maximum path delay calculation.
<code>resistance</code>	The net resistance.
<code>net_list</code>	A list of nets.

---

<code>set_units</code>	<code>[-capacitance cap_unit]</code> <code>[-resistance res_unit]</code> <code>[-time time_unit]</code> <code>[-voltage voltage_unit]</code> <code>[-current current_unit]</code> <code>[-power power_unit]</code>
<code>cap_unit</code>	The capacitance scale factor followed by 'f'.
<code>res_unit</code>	The resistance scale factor followed by 'ohm'.
<code>time_unit</code>	The time scale factor followed by 's'.

<i>voltage_unit</i>	The voltage scale factor followed by 'v'.
<i>current_unit</i>	The current scale factor followed by 'A'.
<i>power_unit</i>	The power scale factor followed by 'w'.

The `set_units` command is used to change the units used by the STA command interpreter when parsing commands and reporting results.

Units are specified as a scale factor followed by a unit name. The scale factors are as follows.

```
M 1E+6
k 1E+3
m 1E-3
u 1E-6
n 1E-9
p 1E-12
f 1E-15
```

An example of the `set_units` command is shown below.

```
set_units -time ns -capacitance pF -current mA -voltage V -resistance kOhm
```

---

**set\_wire\_load\_min\_block\_size size**

The `set_wire_load_min_block_size` command is not supported.

---

**set\_wire\_load\_mode** top|enclosed|segmented

top

enclosed

segmented

The `set_wire_load_mode` command is ignored during timing but is included in SDC files that are written.

---

**set\_wire\_load\_model** -name *model\_name*  
                           [-library *library*]  
                           [-max]  
                           [-min]  
                           [*objects*]

*model\_name* The name of a wire load model.

---

<i>library</i>	Library to look for <i>model_name</i> .
<i>-max</i>	The wire load model is for maximum path delays.
<i>-min</i>	The wire load model is for minimum path delays.
<i>objects</i>	Not supported.

---

<b>set_wire_load_selection_group</b> [-library <i>library</i> ]	
	[-max]
	[-min]
	<i>group_name</i>
	[ <i>objects</i> ]
<i>library</i>	Library to look for <i>group_name</i> .
<i>-max</i>	The wire load selection is for maximum path delays.
<i>-min</i>	The wire load selection is for minimum path delays.
<i>group_name</i>	A wire load selection group name.
<i>objects</i>	Not supported.

The `set_wire_load_selection_group` command is parsed but not supported.

---

<b>source</b>	[-echo] [-verbose] <i>filename</i> > <i>filename</i> >> <i>filename</i> ]
<i>-echo</i>	Print each command before evaluating it.
<i>-verbose</i>	Print each command before evaluating it as well as the result it returns.
<i>filename</i>	The name of the file containing commands to read.

Read STA/SDC/Tcl commands from *filename*.

The `source` command stops and reports any errors encountered while reading a file unless `sta_continue_on_error` is 1.

---

**unset\_case\_analysis** *port\_or\_pin\_list*

*port\_or\_pin\_list* A list of ports or pins.

The `unset_case_analysis` command removes the constant values defined by the `set_case_analysis` command.

---

**unset\_clock\_latency** *[-source] objects*

`-source` Specifies source clock latency (clock insertion delay).

*objects* A list of clocks, pins or ports.

The `unset_clock_latency` command removes the clock latency set with the `set_clock_latency` command.

---

**unset\_clock\_transition** *clocks*

*clocks* A list of clocks.

The `unset_clock_transition` command removes the clock transition set with the `set_clock_transition` command.

---

**unset\_clock\_uncertainty** *[-from|-rise\_from|-fall\_from *from\_clock*] [-to|-rise\_to|-fall\_to *to\_clock*] [-rise] [-fall] [-setup] [-hold] [*objects*]*

*from\_clock*

*to\_clock*

`-rise` The uncertainty is for the rising edge of the clock.

`-fall` The uncertainty is for the falling edge of the clock.

---

<code>-setup</code>	<i>uncertainty</i> is the setup check uncertainty.
<code>-hold</code>	<i>uncertainty</i> is the hold uncertainty.
<i>uncertainty</i>	Clock uncertainty.
<i>objects</i>	A list of clocks, ports or pins.

The `unset_clock_uncertainty` command removes clock uncertainty defined with the `set_clock_uncertainty` command.

---

<b><code>unset_data_check</code></b>	<code>[-from <i>from_object</i>] [-rise_from <i>from_object</i>] [-fall_from <i>from_object</i>] [-to <i>to_object</i>] [-rise_to <i>to_object</i>] [-fall_to <i>to_object</i>] [-setup] [-hold] [-clock <i>clock</i>]</code>
<i>from_object</i>	A pin used as the timing check reference.
<i>to_object</i>	A pin that the setup/hold check is applied to.
<code>-setup</code>	Add a setup timing check.
<code>-hold</code>	Add a hold timing check.
<i>clock</i>	The setup/hold check clock.

The `unset_clock_transition` command removes a setup or hold check defined by the `set_data_check` command.

---

<b><code>unset_disable_inferred_clock_gating</code></b>	
<i>objects</i>	A list of clock gating instances, clock gating pins, or clock enable pins.

The `unset_disable_inferred_clock_gating` command removes a previous `set_disable_inferred_clock_gating` command.

---

<b>unset_disable_timing</b>	<code>[-from <i>from_port</i>] [-to <i>to_port</i>] <i>objects</i></code>
<i>from_port</i>	
<i>to_port</i>	
<i>objects</i>	A list of instances, ports, pins, cells or [library/]cell/port.

The `unset_disable_timing` command is used to remove the effect of previous `set_disable_timing` commands.

---

<b>unset_input_delay</b>	<code>[-rise] [-fall] [-max] [-min] [-clock <i>clock</i>] [-clock_fall] <i>port_pin_list</i></code>
<code>-rise</code>	This is the arrival time for the rising edge of the input.
<code>-fall</code>	This is the arrival time for the falling edge of the input.
<code>-max</code>	This is the minimum arrival time.
<code>-min</code>	This is the maximum arrival time.
<code>clock</code>	The arrival time is from this clock.
<code>-clock_fall</code>	The arrival time is from the falling edge of <code>clock</code>
<code>pin_port_list</code>	A list of pins or ports.

The `unset_input_delay` command removes a previously defined `set_input_delay`.

---

<b>unset_output_delay</b>	<ul style="list-style-type: none"> <li>[-rise]</li> <li>[-fall]</li> <li>[-max]</li> <li>[-min]</li> <li>[-clock <i>clock</i>]</li> <li>[-clock_fall]</li> <li><i>port_pin_list</i></li> </ul>
-rise	This is the arrival time for the rising edge of the input.
-fall	This is the arrival time for the falling edge of the input.
-max	This is the minimum arrival time.
-min	This is the maximum arrival time.
<i>clock</i>	The arrival time is from this <i>clock</i> .
-clock_fall	The arrival time is from the falling edge of <i>clock</i>
<i>pin_port_list</i>	A list of pins or ports.

The `unset_output_delay` command removes a previously defined `set_output_delay`.

---

<b>unset_path_exceptions</b>	<ul style="list-style-type: none"> <li>[-setup]</li> <li>[-hold]</li> <li>[-rise]</li> <li>[-fall]</li> <li>[-from <i>from_list</i>]</li> <li>[-rise_from <i>from_list</i>]</li> <li>[-fall_from <i>from_list</i>]</li> <li>[-through <i>through_list</i>]</li> <li>[-rise_through <i>through_list</i>]</li> <li>[-fall_through <i>through_list</i>]</li> <li>[-to <i>to_list</i>]</li> <li>[-rise_to <i>to_list</i>]</li> <li>[-fall_to <i>to_list</i>]</li> </ul>
-setup	Only apply to setup checks.

<code>-hold</code>	Only apply to hold checks.
<code>-rise</code>	Only apply to rising path edges.
<code>-fall</code>	Only apply to falling path edges.
<code>from_list</code>	A list of clocks, instances, ports or pins.
<code>through_list</code>	A list of instances, pins or nets.
<code>to_list</code>	A list of clocks, instances, ports or pins.

The `unset_path_exceptions` command removes any matching `set_false_path`, `set_multicycle_path`, `set_max_delay`, and `set_min_delay` exceptions.

---

<code>unset_propagated_clock</code>	<i>objects</i>
<i>objects</i>	A list of clocks, ports or pins.

Remove a previous `set_propagated_clock` command.

---

#### `unset_timing_derate`

Remove all derating factors set with the `set_timing_derate` command.

---

<code>update_timing</code>	<code>[-full]</code>
<code>-full</code>	Update all arrivals from scratch (non-incrementally).

The `update_timing` command updates the arrival times for all pins in the design.

---

#### `user_run_time`

Returns the total user cpu run time in seconds as a float.

---

<code>with_output_to_variable</code>	<code>var { commands }</code>
<code>var</code>	The name of a variable to save the output of <code>commands</code> to.
<code>commands</code>	TCL commands that the output will be redirected from.

The `with_output_to_variable` command redirects the output of TCL commands to a variable.

---

<b>write_sdc</b>	<code>[-no_timestamp] [-digits <i>digits</i>] <i>filename</i></code>
<code>-no_timestamp</code>	Do not include a time and date in the SDC file.
<code>digits</code>	The number of digits after the decimal point to report. The default is 4.
<code>filename</code>	The name of the file to write the constraints to.

Write the constraints for the design in SDC format to *filename*.

---

<b>write_sdf</b>	<code>[-corner <i>corner_name</i>] [-divider / .] [-digits <i>digits</i>] [-gzip] [-no_timestamp] [-no_version] <i>filename</i></code>
<code>corner_name</code>	Process corner delays to write.
<code>-divider</code>	Divider to use between hierarchy levels in pin and instance names. Must be '/' or '.'.
<code>digits</code>	The number of digits after the decimal point to report. The default is 4.
<code>-gzip</code>	Write a gzip compressed file.
<code>-no_timestamp</code>	Do not write a DATE statement.
<code>-no_version</code>	Do not write a VERSION statement.
<code>filename</code>	The name of the file to write the constraints to.
<code>digits</code>	The number of digits after the decimal point to report. The default is 4.

Write the delay calculation delays for the design in SDF format to *filename*. The SDF TIMESCALE is same as the `time_unit` in the first liberty file read.

---

<b>write_path_spice</b>	-path_args <i>path_args</i> -spice_directory <i>spice_directory</i> -lib_subckt_file <i>lib_subckts_file</i> -model_file <i>model_file</i> -power <i>power</i> -ground <i>ground</i> <i>path_args</i> -from -through -to arguments as in report_checks.
<i>spice_directory</i>	Spice output directory.
<i>lib_subckts_file</i>	Cell transistor level subckts.
<i>model_file</i>	Transistor model definitions .included by <i>spice_file</i> .
<i>power</i>	Voltage supply name in voltage_map of the default liberty library.
<i>ground</i>	Ground supply name in voltage_map of the default liberty library.

The `write_path_spice` command writes a spice netlist for timing paths. Use `path_args` to specify `-from/-through/-to` as arguments to the `find_timing_paths` command. For each path, a spice netlist and the subckts referenced by the path are written in `spice_directory`. The spice netlist is written in `path_<id>.sp` and subckt file is `path_<id>.subckt`.

The spice netlists used by the path are written to `subckt_file`, which `spice_file` .includes. The device models used by the spice subckt netlists in `model_file` are also .included in `spice_file`. Power and ground names are specified with the `-power` and `-ground` arguments. The spice netlist includes a piecewise linear voltage source at the input and `.measure` statement for each gate delay and pin slew.

## Variables

---

<b>hierarchy_separator</b>	Any character.
----------------------------	----------------

The `hierarchy_separator` separates instance names in a hierarchical instance, net, or pin name. The default value is `'/'`.

---

<b>link_make_black_boxes</b>	0   1
------------------------------	-------

When `link_make_black_boxes` is 1 the `link_design` command will make empty “black box” cells for instances that reference undefined cells. The default value is 1.

---

<b>power_default_signal_toggle_rate</b>	float
---	-------

The toggle rate used to find switching power for non-clock signal. The default value is 0.1.

---

<b>sta_bidirect_net_paths_enabled</b>	0   1
---------------------------------------	-------

When set to 0, paths from bidirectional (inout) ports back through nets are disabled. When set to 1, paths from bidirectional paths from the net back into the instance are enabled. The default value is 0.

---

<b>sta_continue_on_error</b>	0   1
------------------------------	-------

The `source` and `read_sdc` commands stop and report any errors encountered while reading a file unless `sta_continue_on_error` is 1. The default value is 1.

---

<b>sta_crpr_mode</b>	same_pin same_transition
----------------------	--------------------------

When the data and clock paths of a timing check overlap (see `sta_crpr_enabled`), pessimism is removed independent of whether of the path rise/fall transitions. When `sta_crpr_mode` is `same_transition`, the pessimism is only removed if the path rise/fall transitions are the same. The default value is `same_pin`.

---

<b>sta_cond_default_arcs_enabled</b>	0   1
--------------------------------------	-------

When set to 0, default timing arcs with no condition (Liberty timing arcs with no “when” expression) are disabled if there are other conditional timing arcs between the same pins. The default value is 1.

---

<b>sta_crpr_enabled</b>	0   1
-------------------------	-------

During min/max timing analysis for `on_chip_variation` the data and clock paths may overlap. For a setup check the maximum path delays are used for the data and the minimum path delays are used for the clock. Because the gates cannot simultaneously have minimum and maximum delays the timing check slack is pessimistic. This pessimism is known as Common Reconvergent Pessimism Removal, or “CRPR”. Enabling CRPR slows down the analysis. The default value is 1.

---

<b>sta_dynamic_loop_breaking</b>	0   1
----------------------------------	-------

When `sta_dynamic_loop_breaking` is 0, combinational logic loops are disabled by disabling a timing arc that closes the loop. When `sta_dynamic_loop_breaking` is 1, all paths around the loop are reported. The default value is 0.

---

<b>sta_gated_clock_checks_enabled</b>	0   1
---------------------------------------	-------

When `sta_gated_clock_checks_enabled` is 1, clock gating setup and hold timing checks are checked. The default value is 1.

---

<b>sta_input_port_default_clock</b>	0   1
-------------------------------------	-------

When `sta_input_port_default_clock` is 1 a default input arrival is added for input ports that do not have an arrival time specified with the `set_input_delay` command. The default value is 0.

---

<code>sta_internal_bidirect_instance_paths_enabled</code>	0   1
---	-------

When set to 0, paths from bidirectional (inout) ports back into the instance are disabled. When set to 1, paths from bidirectional ports back into the instance are enabled. The default value is 0.

---

<code>sta_propagate_all_clocks</code>	0   1
---------------------------------------	-------

All clocks defined after `sta_propagate_all_clocks` is set to 1 are propagated. If it is set before any clocks are defined it has the same effect as

```
set_propagated_clock [all_clocks]
```

after all clocks have been defined. The default value is 0.

---

<code>sta_propagate_gated_clock_enable</code>	0   1
---	-------

When set to 1, paths of gated clock enables are propagated through the clock gating instances. If the gated clock controls sequential elements setting `sta_propagate_gated_clock_enable` to 0 prevents spurious paths from the clock enable. The default value is 1.

---

<code>sta_recovery_removal_checks_enabled</code>	0   1
--	-------

When `sta_recovery_removal_checks_enabled` is 0, recovery and removal timing checks are disabled. The default value is 1.

---

<code>sta_report_default_digits</code>	integer
--	---------

The number of digits to print after a decimal point. The default value is 2.

---

<code>sta_preset_clear_arcs_enabled</code>	0   1
--	-------

When set to 1, paths through asynchronous preset and clear timing arcs are searched. The default value is 0.

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