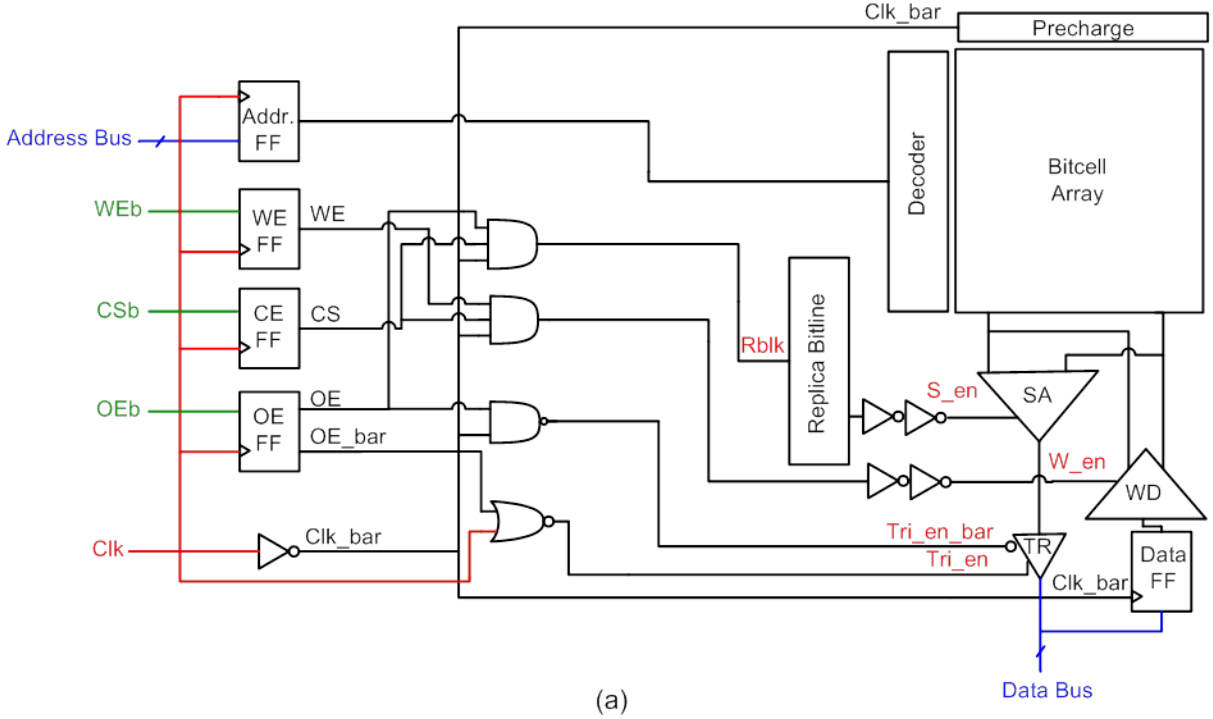
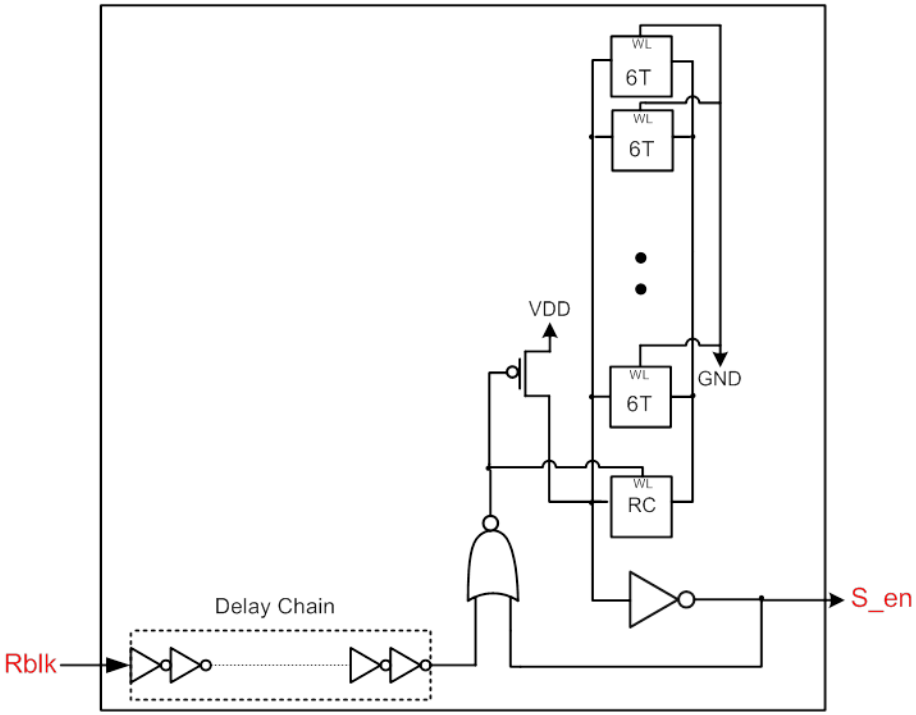

Clk_bar
Precharge
Decoder
Bitcell
Array
Address Bus
Addr.
FF
WEb
WE
FF
WE
CSb
CE
FF
CS
OEb
OE
FF
OE
OE_bar
Clk
Clk_bar
Rblk
Replica Bitline
S_en
SA
W_en
WD
Tri_en_bar
Tri_en
TR
Clk_bar
Data
FF
Data Bus

(a)


WL
6T
WL
6T
VDD
GND
WL
6T
WL
RC
S_en
Delay Chain
Rblk

(b)